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| EXAMINER |
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| BODDIE, WILLIAM |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/707,296 | YANG, HO-HSING | |
| | Examiner | Art Unit | |
| | William L. Boddie | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☒ Claim(s) *1,2,5,7,8,11,15,22,25 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. Figures 4 and 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Information Disclosure Statement*

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

### *Claim Objections*

3. Claims 1, 8, 11, 15, 22 and 25 are objected to because of the following informalities: each claim includes the following phrases, "store a first frame date," and "store a second frame date." Appropriate correction is required.

4. Claims 1, 2, and 7 are objected to because of the following informalities: each claim contains the phrases beginning, “a signal converter”, “wherein said signal converter” and “a signal converter”, respectively. Each phrases is grammatically incorrect and awkward. The inclusion of some grammatical structures to focus which frame data are doing what in the claims is needed. Commas and semi-commas are suggested as possibly ways to amend the current issues. Appropriate correction is required.

5. Claim 5 is objected to because of the following informalities: lines 2 and 4 state, “are integral of the number of bits.” This is awkward and incorrect grammatically. Appropriate correction is required.

6. Claim 27 is objected to because of the following informalities: line 13 states, “is change to a step.” This is awkward and incorrect grammatically. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 14 recites the limitation "said fourth frame" in line 2. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 15 recites the limitations "said eighth frame data" and “said ninth frame data" in the last phrase. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 29 recites the limitation "said eleventh frame data" in the second phrase. There is insufficient antecedent basis for this limitation in the claim.

11. Claims 1-6 and 8-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. As to independent claim 1, it is unclear as to how the second frame data corresponds to the first frame data as stated in the last few lines of the claim. Additionally, the discussion of the multiplexer unit is unclear as to its operation with respect to the second frame data. Currently it appears as though the multiplexer transmits the outputted second frame data to the buffer, which is supposed to output the second frame data.

13. With respect to claim 2, claim 2 requires that a first data latch receive a fourth frame and output the first frame. Additionally, a second data latch receives a fifth frame and outputs the second frame. This is inconsistent with the previous independent claim and figure 6. Here again there are issues with where the second data frame is being outputted.

14. With respect to claim 8, claim 8 suffers from the same language discussed above in claim 2.

15. With respect to claim 9, claim 9 states that, the motion picture enhancing unit compares the second frame data to the second frame data. It seems the Applicant might have intended to compare the second and third frame data.

16. Claims 11-12 contain the same grammatical and indefinite issues as those shown above in claims 1-2.

17. Claims 15 and 21 state "a signal converter, in response to said first frame data." This initial phrase is unclear as to how it is supposed to be interpreted. In short the action that the signal converter is supposed to perform is unclear.

18. Claims 15 and 21 also in disclosing the second data flow switcher states that the output is either 8th and 9th or 8th and 9th respectively. It is unclear what the difference is between these two options.

19. Claims 15, 21 and 25 also contain the same multiplexer unit language discussed above in claim 1.

20. Claim 16 contains several places within the claim where the position of frames previously labeled in claim 15 are directly contradicted. The first instance of this is discussion of the first data flow switcher that claim 16 states outputs a tenth and third frame. This directly contradicts claim 15, which states that the first data flow switcher outputs a first and third frame. Additionally the signal converter receives the tenth, third and the eleventh frames in claim 16. This again contradicts claim 15, which states the signal converter receives a first, third and second frame.

21. These contradictions are also present in claims 17, and 26-30, each which relabels the frames once again.

22. Those claims not specifically discussed above are rejected by virtue of their dependence upon their individual indefinite independent claim.

23. *It is suggested by the Examiner that the Applicants label the claimed frames with the labels for the frames in figures 6 and 7 as appropriate. This would likely ensure that all the frames are kept in order and manageable.*

***Claim Rejections - 35 USC § 102***

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

25. Claims 1, 6, 15 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Asma (US 6,489,964). It should be noted that Van Asma also qualifies as prior art under 35 U.S.C. 102(a).

**With respect to claim 1,** Van Asma discloses, a circuit for enhancing motion picture quality, comprising:

a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a first frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said first frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO2), and first-in-first-out outputting said second frame data (output of FIFO2); said first frame data being shown in a motion picture after said second frame data (clear from fig. 3);

a frame memory, for storing a motion picture data (SDRAM in fig. 3);

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required); and

a signal converter (LUT in fig. 3), for obtaining a compensation data to output a third frame data (output of LUT in fig. 3) in response to said first frame data and said second frame data corresponding to said first frame data (clear from fig. 3).

**With respect to claim 6,** Van Asma discloses, the circuit of claim 1 (see above), wherein said circuit is applied to a liquid crystal display (col. 4, lines 53-56).

**With respect to claim 15,** Van Asma discloses, a circuit for enhancing motion picture quality, comprising:

a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a first frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said first frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO2), and first-in-first-out outputting said second frame data (output of FIFO2); said first frame data being shown in a motion picture after said second frame data (clear from fig. 3);

a frame memory, for storing a motion picture data (SDRAM in fig. 3);

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required); and

a signal converter (LUT in fig. 3) in response to said first frame data, a third frame data and said second frame data corresponding to said third frame data, for obtaining a compensation data to output a fourth frame data (first output of LUT) and a fifth frame data (subsequent output of LUT);

a first data flow switcher (input line memory in fig. 4), for receiving a sixth frame data (first input into "lin mem" in fig. 4) and a seventh frame data (subsequent input into "lin mem" in fig. 4) and transforming said sixth frame data and seventh frame data into one of said first frame data and said third frame data respectively and said third frame data and said first frame data respectively (sequential outputs of "lin mem" in fig. 4); and

a second data flow switcher (DA in fig. 4), for receiving said fourth frame data and said fifth frame data and transforming said fourth frame data and fifth frame data into one of said eighth frame data and said ninth frame data respectively and said eighth frame data and said ninth frame data respectively (sequential outputs of DA in fig. 4).

**With respect to claim 20,** Van Asma discloses, the circuit of claim 15 (see above), wherein said circuit is applied to a liquid crystal display (col. 4, lines 53-56).

26. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Lei (US 6,130,911).

**With respect to claim 7,** Lei discloses, a circuit for enhancing motion picture quality, comprising:

a nonlinear quantizer (72 in fig. 4) receiving a first frame data (input of 72) and quantizing said first frame data by using a nonlinear quantization method to output a second frame data (output of 72);

a frame memory module (100 in fig. 4), coupled to said nonlinear quantizer, for receiving said second frame data (input of 100) and outputting a third frame data (output of 100) corresponding to said second frame data, said second frame data being shown in a motion picture after said third frame data (clear from fig. 4); and

a signal converter (80 in fig. 4), in response to said second frame data and said third frame data corresponding to said second frame data, for obtaining a compensation data (output of 80) to compensate said first frame data for outputting a fourth frame data.

***Claim Rejections - 35 USC § 103***

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 1-5, 8-19 and 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lei (US 6,130,911) in view of Van Asma (US 6,489,964).

**With respect to claim 1,** Lei discloses, a circuit for enhancing motion picture quality (fig. 4), comprising:

a frame memory, for storing a motion picture data (78 in fig. 4);

a signal converter (70 in fig. 4), for obtaining a compensation data to output a third frame data (output of 70 in fig. 4) in response to said first frame data and said second frame data corresponding to said first frame data.

Lei does not expressly disclose, including buffers and a multiplexer in the circuit.

Van Asma discloses, a circuit for simplifying display circuitry, comprising:

a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a first frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said first frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO2), and first-in-first-out outputting said second frame data (output of FIFO2); said first frame data being shown in a motion picture after said second frame data (clear from fig. 3);

a frame memory, for storing a motion picture data (SDRAM in fig. 3);

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace small frame memory of Lei with the frame buffer of Van Asma.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

**With respect to claim 2,** Lei and Van Asma disclose, the circuit of claim 1 (see above).

Lei further discloses, a first data latch (76 in fig. 4), for receiving a fourth frame data (input of 76) and outputting said first frame data, the number of bits of said first frame data is larger than the number of bits of said fourth frame data (col. 4, lines 55-61, for example);

a second data latch (82 in fig. 4), for receiving a fifth frame data (input of 82) and outputting said second frame data, the number of bits of said second frame data is larger than the number of bits of said fifth frame data (col. 6, line 45 for example);

wherein said signal converter (70 in fig. 4) is for obtaining said compensation data to output said third frame data in response to said fourth frame data and said fifth frame data corresponding to said second frame data (clear from fig. 4).

**With respect to claim 3,** Lei and Van Asma disclose, the circuit of claim 2 (see above).

Lei further discloses, a nonlinear quantizer (72 in fig. 4) receiving a sixth frame data (input of 72 in fig. 4) and quantizing said sixth frame data by using a nonlinear quantization method to output said fourth frame data (output of 72; input of 76), said signal converter receiving said sixth frame data (input of 70 in fig. 4) and compensating said sixth frame data based on said compensation data to obtain said third frame data (clear from fig. 4).

**With respect to claim 4,** Lei and Van Asma disclose, the circuit of claim 3 (see above).

Lei further discloses, a motion picture enhancing unit (80 in fig. 4), for simultaneously receiving said fourth frame data and said fifth frame data and comparing said fourth frame data and said fifth frame data to generate said compensation data based on the difference between said fourth frame data and said fifth frame data (col. 1, lines 50-54; col. 6, lines 33-34); and

a data processing unit (70 in fig. 4), for simultaneously receiving said sixth frame data and said compensation data corresponding to said sixth frame data, and compensating said sixth frame data based on said compensation data to obtain said third frame data (col. 6, lines 50-52).

**With respect to claim 5,** Lei and Van Asma disclose, the circuit of claim 2 (see above).

Lei further discloses, wherein the number of bits of said first frame data are integral of the number of bits of said fourth frame data, and the number of bits of said

second frame data are said integral of the number of bits of said fifth frame data (col. 7, lines 57-59).

**With respect to claim 8,** Lei discloses, the circuit of claim 7 (see above), wherein said frame memory module comprises:

a frame memory (78 in fig. 4).

Lei does not expressly disclose including buffers and a multiplexer in the frame memory module.

Van Asma discloses, a circuit for simplifying display circuitry, comprising:

a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said second frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a third frame data (input of FIFO2), and first-in-first-out outputting said third frame data (output of FIFO2);

a frame memory, for storing a motion picture data (SDRAM in fig. 3); and

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory,

for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said third frame data to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace small frame memory of Lei with the frame buffer of Van Asma.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

**With respect to claim 9,** Lei and Van Asma disclose, the circuit of claim 8 (see above).

Lei further discloses, a motion picture enhancing unit (80 in fig. 4), for simultaneously receiving said third frame data and said second frame data and comparing said second frame data and said second frame data to generate said compensation data based on the difference between said second frame data and said third frame data (col. 1, lines 50-54; col. 6, lines 33-34); and

a data processing unit (70 in fig. 4), for simultaneously receiving said first frame data and said compensation data corresponding to said first frame data, and compensating said first frame data based on said compensation data to obtain said fourth frame data (col. 6, lines 50-52).

**With respect to claim 10,** Lei and Asma disclose, the circuit of claim 8 (see above).

Lei does not expressly disclose, wherein said circuit is applied to a liquid crystal display.

Asma further discloses, wherein said circuit is applied to a liquid crystal display (col. 4, lines 53-56).

It would have been obvious to one of ordinary skill in the art to use the circuit of Lei in a liquid crystal display as taught by Asma, due to the well-known slow response of liquid crystal displays which makes them especially susceptible to motion artifacts.

**With respect to claims 11-14,** Lei and Asma disclose, the circuit of claims 1-4 (see above). As claims 11-14 are merely method versions of these claims, they are rejected on the same merits shown above in the rejections of claims 1-4.

**With respect to claim 15,** Lei discloses, a circuit for enhancing motion picture quality (fig. 4), comprising:

a frame memory, for storing a motion picture data (78 in fig. 4);

a signal converter (70 in fig. 4) in response to said first frame data, a third frame data and said second frame data corresponding to said third frame data, for obtaining a compensation data to output a fourth frame data (first output of 70) and a fifth frame data (subsequent output of 70);.

Lei does not expressly disclose, including buffers, data flow switchers and a multiplexer in the circuit.

Van Asma discloses, a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a first frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said first frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO2), and first-in-first-out outputting said second frame data (output of FIFO2); said first frame data being shown in a motion picture after said second frame data (clear from fig. 3);

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory, for selecting and transmitting one of said outputted said first frame data to said frame memory and said outputted said second frame data to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required); and

a first data flow switcher (input line memory in fig. 4), for receiving a sixth frame data (first input into "lin mem" in fig. 4) and a seventh frame data (subsequent input into "lin mem" in fig. 4) and transforming said sixth frame data and seventh frame data into one of said first frame data and said third frame data respectively and said third frame data and said first frame data respectively (sequential outputs of "lin mem" in fig. 4); and

a second data flow switcher (DA in fig. 4), for receiving said fourth frame data and said fifth frame data and transforming said fourth frame data and fifth frame data into one of said eighth frame data and said ninth frame data respectively and said eighth frame data and said ninth frame data respectively (sequential outputs of DA in fig. 4).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace small frame memory of Lei with the frame buffer of Van Asma and include the frame buffers of Van Asma.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

**With respect to claim 16,** Lei and Van Asma disclose, the circuit of claim 15 (see above).

Lei, when combined with Van Asma as shown above, further discloses, a first data latch (76 in fig. 4), coupled to and between said first data flow switcher and said first dual-port buffer, said first data flow receiving said sixth frame data and seventh frame data, and transforming said sixth frame data and said seventh frame data into one of a tenth frame data and said third frame data respectively and said third frame data and said tenth frame data respectively, said first data latch, for receiving said tenth frame data (input of 76) and outputting said first frame data, the number of bits of said first frame data is larger than the number of bits of said tenth frame data (col. 4, lines 55-61, for example);

a second data latch (82 in fig. 4), coupled to and between said first dual-port buffer and said signal converter, for receiving said second frame data (input of 82) and outputting an eleventh frame data, the number of bits of said second frame data is larger than the number of bits of said eleventh frame data (col. 6, line 45 for example);

wherein said signal converter (70 in fig. 4), in response to said tenth frame data, said third frame data and said eleventh frame data corresponding to said third frame data obtains said compensation data to output said fourth frame data and said fifth frame data (clear from fig. 4).

**With respect to claim 17,** Lei and Van Asma disclose, the circuit of claim 16 (see above).

Lei, when combined with Van Asma as shown above, further discloses a first nonlinear quantizer (72 in fig. 4), coupled to and between said first data flow switcher and said first data latch, said first data flow switcher receiving said sixth frame data and seventh frame data, and transforming said sixth frame data and said seventh frame data into one of a twelfth frame data and said third frame data respectively and said third frame data and said twelfth frame data respectively, said first nonlinear quantizer receiving said twelfth frame data (input of 72 in fig. 4) and quantizing said twelfth frame data by using a nonlinear quantization method to output said tenth frame data (output of 72; input of 76); and

a second nonlinear quantizer (66 in fig. 4), coupled to and between said first data flow switcher and said signal converter, for receiving said third frame data (input of 72 in fig. 4) and quantizing said third frame data by using a nonlinear quantization method to output said thirteenth frame data (output of 72; input of 76);

wherein said signal converter, in response to said twelfth frame data, said third frame data, and said thirteenth frame data corresponding to said eleventh frame data (input of 70 in fig. 4) obtains said compensation data to output said fourth frame data and said fifth frame data (clear from fig. 4).

**With respect to claim 18,** Lei and Van Asma disclose, the circuit of claim 17 (see above).

Lei further discloses, a motion picture enhancing unit (80 in fig. 4), for simultaneously receiving said thirteenth frame data and said eleventh frame data and comparing said thirteenth frame data and said eleventh frame data to generate said compensation data based on the difference between said thirteenth frame data and said eleventh frame data (col. 1, lines 50-54; col. 6, lines 33-34); and

a first data processing unit (70 in fig. 4), for simultaneously receiving said twelfth frame data and said compensation data corresponding to said twelfth frame data, and compensating said twelfth frame data based on said compensation data to obtain said fourth frame data (col. 6, lines 50-52)

a second data processing unit (68 in fig. 4), for simultaneously receiving said third frame data and said compensation data corresponding to said third frame data, and compensating said third frame data based on said compensation data to obtain said fifth frame data (col. 6, lines 50-52).

**With respect to claim 19,** Lie and Van Asma disclose, the circuit of claim 16 (see above).

Lei further discloses, wherein the number of bits of said first frame data are integral of the number of bits of said tenth frame data, and the number of bits of said second frame data are said integral of the number of bits of said eleventh frame data (col. 7, lines 57-59).

**With respect to claim 21,** Lei discloses, a first nonlinear quantizer (72 in fig. 4), for receiving a first frame data (input of 72 in fig. 4) and quantizing said first frame data

by using a nonlinear quantization method to output said second frame data (output of 72; input of 76); and

a second nonlinear quantizer (66 in fig. 4), for receiving said third frame data (input of 72 in fig. 4) and quantizing said third frame data by using a nonlinear quantization method to output said fourth frame data (output of 72; input of 76);

a frame memory module (100 in fig. 4), coupled to said first nonlinear quantizer, receiving said second frame data and outputting a fifth frame data (output of 84) corresponding to said second frame data, said second frame data being shown in a motion picture after said fifth frame data (clear from fig. 4);

a signal converter (68, 70, 80 in fig. 4), in response to said first frame data, said third frame data, said fourth frame data and said fifth frame data corresponding to said fourth frame data, for obtaining a compensation data to output a sixth frame data (output of 68) and a seventh frame data (output of 80).

Lei does not expressly disclose, including data flow switchers in the circuit.

Van Asma discloses, a first data flow switcher (input line memory in fig. 4), for receiving a eighth frame data (first input into “lin mem” in fig. 4) and a ninth frame data (subsequent input into “lin mem” in fig. 4) and transforming said eighth frame data and ninth frame data into one of said first frame data and said third frame data respectively and said third frame data and said first frame data respectively (sequential outputs of “lin mem” in fig. 4); and

a second data flow switcher (DA in fig. 4), for receiving said sixth frame data and said seventh frame data and transforming said sixth frame data and seventh frame data

into one of said tenth frame data and said eleventh frame data respectively and said tenth frame data and said eleventh frame data respectively (sequential outputs of DA in fig. 4).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the frame buffers of Van Asma in the circuit of Lei.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

**With respect to claim 22,** Lei discloses, the circuit of claim 21 (see above), wherein said frame memory module comprises:

a frame memory (78 in fig. 4).

Lei does not expressly disclose including buffers and a multiplexer in the frame memory module.

Van Asma discloses, a circuit for simplifying display circuitry, comprising:

a first dual-port buffer (FIFO1 in fig. 3), for receiving and temporarily storing a second frame data (input of FIFO1 in fig. 3), and first-in-first-out outputting said second frame data (output of FIFO1);

a second dual-port buffer (FIFO2 in fig. 3), for receiving and temporarily storing a fifth frame data (input of FIFO2), and first-in-first-out outputting said fifth frame data (output of FIFO2);

a frame memory, for storing a motion picture data (SDRAM in fig. 3); and

a multiplexer unit (memcontr in fig. 3) coupled to said first dual-port buffer, said second dual-port buffer, and said frame memory,

for selecting and transmitting one of said outputted said second frame data to said frame memory and said outputted said third frame data to said second dual-port buffer (clear from fig. 3 that the memcontr is connected as required).

Lei and Van Asma are analogous art because they from the same field of endeavor namely, display memory control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace small frame memory of Lei with the frame buffer of Van Asma.

The motivation for doing so would have been to simplify the circuitry and generate a more integrated design requiring less clock signals (Van Asma; col. 2, lines 1-5).

**With respect to claim 23,** Lei and Van Asma disclose, the circuit of claim 22 (see above).

Lei further discloses, a motion picture enhancing unit (80 in fig. 4), for simultaneously receiving said fourth frame data and said fifth frame data and comparing said fourth frame data and said fifth frame data to generate said compensation data based on the difference between said fourth frame data and said fifth frame data (col. 1, lines 50-54; col. 6, lines 33-34); and

a first data processing unit (70 in fig. 4), for simultaneously receiving said first frame data and said compensation data corresponding to said twelfth frame data, and

compensating said twelfth frame data based on said compensation data to obtain said fourth frame data (col. 6, lines 50-52)

a second data processing unit (68 in fig. 4), for simultaneously receiving said third frame data and said compensation data corresponding to said third frame data, and compensating said third frame data based on said compensation data to obtain said fifth frame data (col. 6, lines 50-52).

**With respect to claim 24,** Lei and Asma disclose, the circuit of claim 21 (see above).

Lei does not expressly disclose, wherein said circuit is applied to a liquid crystal display.

Asma further discloses, wherein said circuit is applied to a liquid crystal display (col. 4, lines 53-56).

It would have been obvious to one of ordinary skill in the art to use the circuit of Lei in a liquid crystal display as taught by Asma, due to the well-known slow response of liquid crystal displays which makes them especially susceptible to motion artifacts.

**With respect to claims 25-30,** Lei and Asma disclose, the circuit of claims 15-20 (see above). As claims 11-14 are merely method versions of these claims, they are rejected on the same merits shown above in the rejections of claims 15-20.

***Conclusion***

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will L. Boddie whose telephone number is (571) 272-

0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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wlb
6/21/07

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